AMENDMENTS

IN THE CLAIMS

Please amend the claims as follows:

13. (Twice Amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of salicide material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal, forming salicided layers comprising reacted salicide material over the surface of said source and drain implants;

first removing un-reacted salicide material from the surface of said substrate;

depositing an isolation film over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of filler material over the surface of said isolation film to a thickness such that the surface of said layer of filler material extends above the surface of said isolation film even where said isolation film overlays the surface of said at least one gate electrode;

polishing the surface of said layer of filler material and said layer of isolation film down to the surface of said layer of boronitride of said at least one gate electrode, using said layer of boronitride as a stop for said process of polishing, advantageously using a polishing rate of filler material that is larger than a polishing rate of boronitride, said layer of boronitride providing a save stop for said polishing the surface of the layer of filler material and the layer of isolation film, thereby further preventing corrosion of the surface of said at least one gate electrode;

removing said layer of boronitride from said at least one gate electrode, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over the surface of said polished layer of filler material, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material, a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing un-reacted salicide material from the surface of said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

REMARKS

Examiner Maria F. Guerrero is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested. Claims 13-24 are pending.